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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,624	07/15/2003	Noboru Matsuda	240349US2TTCCONT	5650

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EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,624	MATSUDA ET AL.	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12,14-18 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12,14-18 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/667,559.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-12 and 14-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Inoue et al (US. 5,714,775).

Regarding claim 1, Inoue (Figs. 13-14) discloses a semiconductor device comprising: a first gate electrode group 35 (column 11, lines 14-15) having a plurality of gate electrodes 37 formed on a semiconductor substrate to be away from each other at first equal spacing (column 10, lines 58-59); a first gate insulating film 36 formed on both of the sidewall-surfaces opposed to each other of a first gate electrode 37 of the first gate electrode group 35; a channel region formed along the gate insulating film 36 on both of the sidewall-surfaces opposed to each other of the first gate electrode 37 of the first gate electrode group 35 (column 10, lines 59-61); a source diffused layer 38 between first gate electrodes 37 of the first gate electrode group; a source contact having a portion 42 (rightmost portion of the contact) formed separated from the first gate electrode 37 (leftmost gate electrode 37) of the first gate electrode group 35 by a second spacing greater than the first spacing; and source regions 34/45 for electrically interconnecting the first gate electrode group 35 and the source contact (column 10, lines 58-61).

Regarding claims 2-3, Inoue (Figs. 13-14) discloses a semiconductor device comprising: a first gate electrode group 35 (column 11, lines 14-15) having a plurality of gate electrodes 37 formed on a semiconductor substrate to be away from each other at first equal spacing (column 10, lines 58-59); a first gate insulating film 36 formed on both of sidewall-surfaces opposed to each other of a first gate electrode 37 of the first gate electrode group 35; a channel region formed along the gate insulating film 36 on both of the sidewall-surfaces opposed to each other of the first gate electrode 37 of the first gate electrode group 35 (column 10, lines 59-61); a source contact portion 42 (rightmost portion of source contact) formed separated from the first gate electrode 35 to be away from the first gate electrode group 35 at a second spacing; and source regions 38 for electrically interconnecting the first gate electrode group 35 and the source contact portion 42, wherein the source regions 38 are electrically connected to each other at one end of the first gate electrode group 35 (top end) by the source contact 42, and separated from each other at the other end of the first gate electrode group 35 (bottom end).

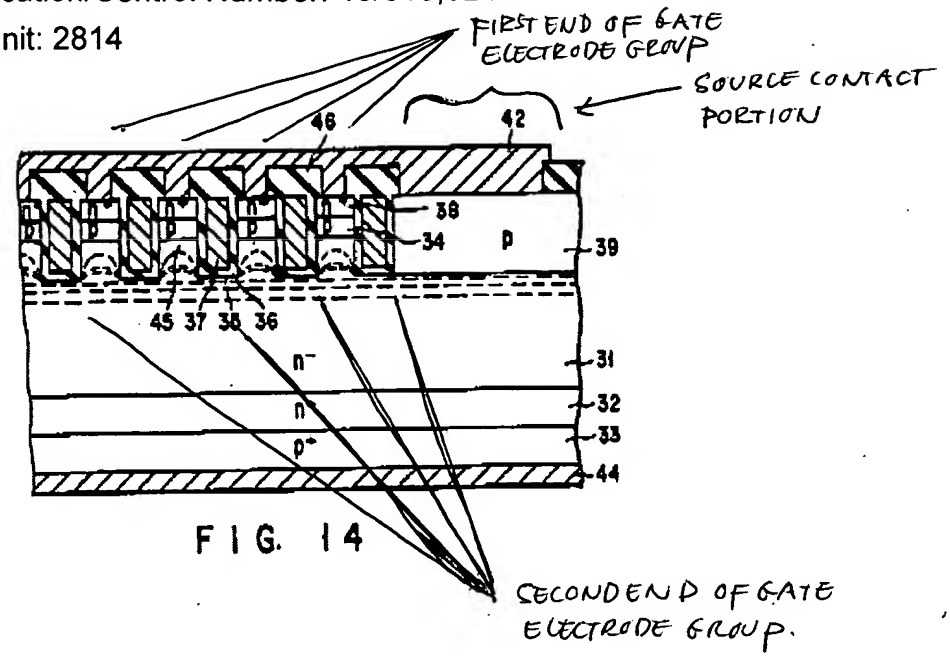

FIG. 14

Regarding claim 4, Inoue (Figs. 13-14) discloses a semiconductor device comprising: a first gate electrode group 35 (see cross section in Fig. 14) having a plurality of gate electrodes 37 formed on a semiconductor substrate to be away from each other at first equal spacing (column 10, lines 58-59); a first gate insulating film 36 formed on both of sidewall-surfaces opposed to each other of a first gate electrode 37 of the first gate electrode group 35; a first channel region formed along the gate insulating film 36 on both of the sidewall-surfaces opposed to each other of the first gate electrode 37 of the first gate electrode group 35 (column 10, lines 59-61); a first source diffused layer 38 between first gate electrodes 37 of the first gate electrode group; a second gate electrode group 35 separated from the first gate electrode 35 (see Fig. 13) and having a plurality of gate electrodes 37 formed on the substrate to be away from each other at the first equal spacing (Fig. 14); a second gate insulating film 36 formed on both of sidewall-surfaces opposed to each other of a first gate electrode 37 of the second gate electrode group 35; a second channel region formed along the gate insulating film 36 on

both of the sidewall-surfaces opposed to each other of the first gate electrode 37 of the second gate electrode group 35 (column 10, lines 59-61); a second source diffused layer 38 between first gate electrodes 37 of the second gate electrode group; a source contact portion 42 (rightmost portion of source contact) formed separated between the first and second gate electrode groups 35 (see Fig. 13) to be away from the first and second gate electrode groups at a second spacing; and source regions 34/45 for electrically interconnecting the first gate electrode group 35 and the source contact portion 42, wherein the source regions 34/45 are connected to each other at one end of the first gate electrode group 35 (bottom end), and separated from each other at the other end of the first gate electrode group (top end).

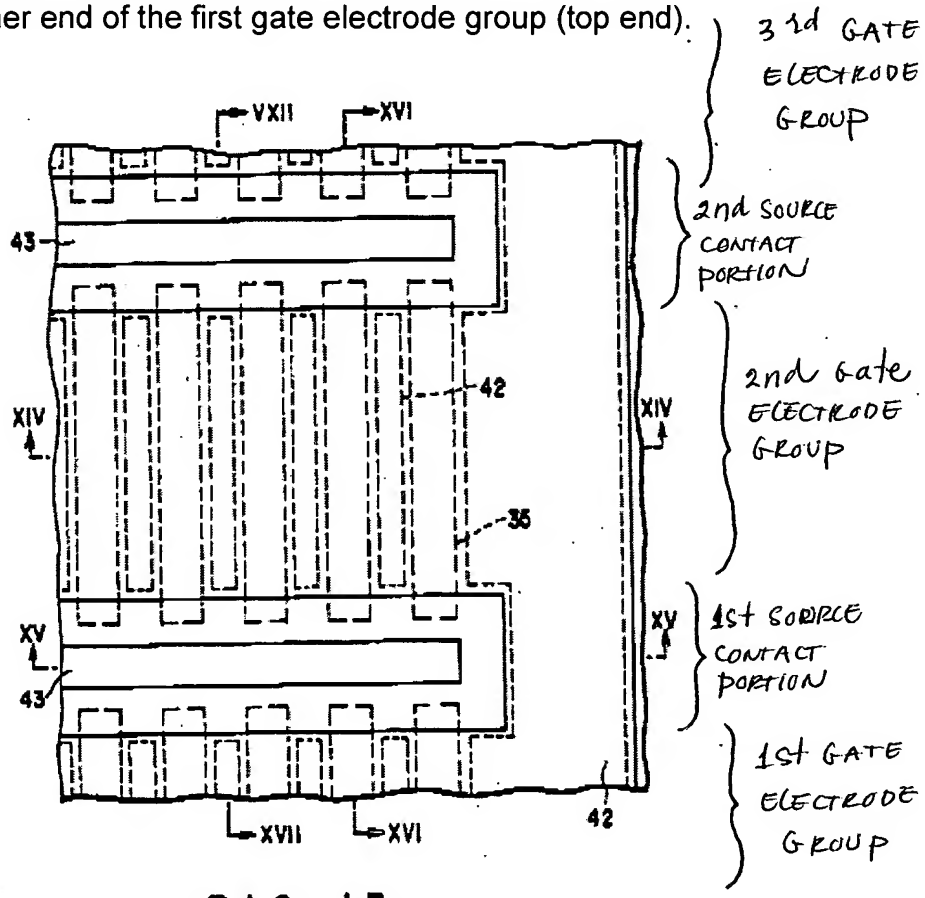

FIG. 13

Regarding claims 5-8 and 10, Inoue (Fig. 14) further discloses that the first and second gate electrode groups 35 are formed in trench structures, the gate electrodes 37 of the first group 35 are electrically connected to each other at the other end (see Fig. 12), and all of the gate electrodes 37 of the first gate electrode group 35 are used as gates for a MOS transistor.

Regarding claim 9, Inoue (Fig. 14) further discloses a source electrode on the semiconductor substrate, wherein the source contact portion 42 is an electrode drawn from the source electrode.

Regarding claim 11, Inoue (Figs. 13-14) discloses a semiconductor device comprising: a first gate electrode group 35 (see bottom group 35 in Fig. 13) having a plurality of gate electrodes 37 formed on a semiconductor substrate to be away from each other at first equal spacing (Fig. 14 and column 10, lines 58-59); a first gate insulating film 36 formed on both of sidewall-surfaces opposed to each other of a first gate electrode 37 of the first gate electrode group 35; a first channel region formed along the gate insulating film 36 on both of the sidewall-surfaces opposed to each other of the first gate electrode 37 of the first gate electrode group 35 (column 10, lines 59-61); a first source diffused layer 38 between first gate electrodes 37 of the first gate electrode group; a second gate electrode group 35 (see center group 35 in Fig. 13) having a plurality of gate electrodes 37 on the substrate to be away from each other at the first equal spacing (Fig. 14 and column 10, lines 58-59); a second gate insulating film 36 formed on both of sidewall-surfaces opposed to each other of a first gate

electrode 37 of the second gate electrode group 35; a second channel region formed along the gate insulating film 36 on both of the sidewall-surfaces opposed to each other of the first gate electrode 37 of the second gate electrode group 35 (see top group 35 in Fig. 13); a second source diffused layer 38 between first gate electrodes 37 of the second gate electrode group 35; a third gate electrode group 35 having a plurality of gate electrodes 37 formed on the substrate to be away from each other at the first equal spacing (Fig. 14 and column 10, lines 58-59); a third gate insulating film 36 formed on both of sidewall-surfaces opposed to each other of a first gate electrode 37 of the third gate electrode group 35; a third channel region formed along the gate insulating film 36 on both of the sidewall-surfaces opposed to each other of the first gate electrode 37 of the third gate electrode group 35 (column 10, lines 59-61); a third source diffused layer 38 between first gate electrodes 37 of the third gate electrode group 35; a first source contact portion 42 (see rightmost portion of source contact 42 in Fig. 13) formed between the first and second gate electrode groups 35 to be away from the first and second gate electrode groups 35 at a second spacing; a second source contact portion 42 (also see rightmost portion of source contact 42 in Fig. 13) formed between the second and third gate electrode groups 35 to be away from one selected from the second and third gate electrode groups 35 at the second spacing; first source regions 34/45 which electrically interconnect the first gate electrode group 35 and the first source contact portion 42; and second source regions 34/45 which electrically interconnect the second gate electrode group 35 and the second source contact portion 42, wherein the first source regions 34/45 are connected to each other at one end of the

first gate electrode group 35 (bottom end) and are separated from each other at the other end of the first gate electrode group (top end), and the second source regions 34/45 are connected to each other at one end of the second gate electrode group (bottom end) and are separated from each other at the other end of the second gate electrode group (top end).

Regarding claims 12, 14 and 15, Inoue further discloses that the first and second gate electrode groups 35 are formed in trench structures (Fig. 14) and are connected to each other at the other end by rightmost source contact 42 (see Fig. 13), and each of the first and second source regions 38 is a diffused layer formed on the substrate.

Regarding claims 16 and 18, Inoue (Fig. 13) further discloses that the first source contact portion 42 and the first gate electrode group 35 constitute one MOS transistor, and the second source contact portion 42 and the second gate electrode group 35 constitute another MOS transistor.

Regarding claim 17, Inoue (Fig. 14) also discloses that each of the first and second source contact portions is an electrode 42 drawn from a source electrode, and these portions are connected to each other.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Inoue et al (US. 5,714,775).

Inoue does not disclose that the rightmost source contact portion 42 is away from the gate electrode group 35 at a second spacing greater than the first spacing formed between the gate electrodes 37.

However, it has been held that, where the only different between the prior art and the claims was a recitation of relative dimensions of the claimed device and a device having the claimed relative dimensions would not perform differently than the prior art device, the claimed device was not patentably distinct from the prior art device. *In Gardner v. TEC Systems, Inc.*, 725 F. 2d 1338, 220 USPQ 777 (Fed. Cir. 1984), Cert. Denied, 469 U.S. 830, 225 USPQ 232 (1984). Therefore, it would have been obvious to form the rightmost source contact portion 42 (Fig. 14) away from the gate electrode group 35 at a second spacing greater than the first spacing formed between the gate electrodes because it appears that these changes would produce no functional differences.

Response to Arguments

5. Applicant argues that figure 14 of Inoue does not teach both "a source diffused layer" and "source regions" as amended.

This argument is not persuasive because figure 14 of Inoue clearly teaches both source diffused layers 38 and source regions 34/45. The source region 34/45 includes the source-diffused layer 38 and electrically interconnects the first gate electrode 37 and

the source contact 42 (column 10, lines 58-63). Therefore, figure 14 of Inoue does suggest the invention as claimed.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC
September 14, 2006

PHAT X. CAO
PRIMARY EXAMINER